Docket No.: M4065.0967/P967

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

DOUBLE THROUGHPUT ANALOG TO DIGITAL CONVERTER

Inventors

Ali E. Zadeh
Lin Ping Ang

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 828-2232

DOUBLE THROUGHPUT ANALOG TO DIGITAL CONVERTER

FIELD OF INVENTION

[0001] The present invention relates generally to analog to digital conversion, and more particularly, to a double throughput analog to digital converter.

BACKGROUND OF THE INVENTION

[0002] Analog integrated circuits (ICs) are integrated circuits that process analog signals. Examples of such circuits include, for example, amplifiers, reference current sources, and reference voltage sources. Analog ICs often require the use of, and constantly consume, a DC bias current. Digital integrated circuits are ICs which process digital signals. Examples of digital integrated circuits include, for example, logical circuit and state machines, such as processors. Digital circuits with complementary metal oxide semiconductor (CMOS) logic generally do not use a DC bias current.

[0003] Some integrated circuits, however, process both analog and digital signals. Such circuits are known as mixed signal integrated circuits. Mixed signal ICs generally require the use of a DC bias current supply. A common example of a mixed signal circuit is an analog-to-digital converter (ADC). ADCs accept an input analog signal and produce an output digital signal having a value corresponding to the magnitude of the input analog signal. ADCs are found in numerous products, including a variety of portable electronic devices, such as CMOS based imaging products. Many CMOS based imaging products include ICs that include a plurality of ADCs, so that a plurality of analog signals can be simultaneously converted to corresponding digital signals. Since portable electronic devices are generally battery powered, it is desirable to reduce the power consumption of mixed signal ICs, such as those ICs which include ADCs.

[0004] Fig. 1 illustrates general features of a conventional pipelined ADC 100. ADC 100 comprises a clock generator 110, a reference voltage source 120, a plurality of cascaded identical stages 101, and a digital block 130. The digital block 130 provides N output bits, one for each of stages 101.

[0005] Now also referring to Fig. 3, it can be seen that the clock generator 110 accepts a clock signal ϕ and produces two non-overlapping clock signals ϕ 1 and ϕ 2. The two clock signals ϕ 1 and ϕ 2 are generated so that they define distinct phases for each clock cycle of the original clock signal ϕ. In each stage 101 of a typical ADC 100, different tasks are performed during the different phases defined by clock signals ϕ 1 and ϕ 2. For example, in each odd stage 101 (e.g., a first, third, fifth, etc. stage of the ADC 100), when clock signal ϕ 1 is high, the stage 101 is in a sampling phase, and when clock signal ϕ 2 is high, the stage 101 is in a conversion phase. Each adjacent phase utilizes the clock signals ϕ 1 and ϕ 2 in a complementary fashion. Thus, in the above example, each even stage 101 (e.g., a second, fourth, sixth, etc. stage 101 of the ADC 100) is in a conversion phase when clock signal ϕ 1 is high and each even stage is in a sampling phase when clock signal ϕ 2 is high. The reference voltage generator 120 accepts a power signal from the power supply (not illustrated) and outputs a reference voltage signal Vref. The two clock signals ϕ1, ϕ2 and the reference voltage signal are supplied to each stage 101.

[0006] Each stage 101 accepts an input signal and outputs an output signal. The stages 101 are cascaded, so that the first stage 101 accepts an input signal at terminal 150 and outputs a signal which becomes the input signal for the next stage; and so forth. More specifically, when clock signals ϕ1 or ϕ2 corresponds to a sampling phase of a given stage 101 of the ADC 100, the input signal of each stage 101 is distributed to processing block 103 and a first input terminal for amplifier block 102.

[0007] Processing block 103 implements the well known process of performing an analog-to-digital conversion of the input signal and generating an analog signal corresponding to the (partially) converted digital signal. The generated analog signal, when presented as an input signal to amplifier 215 of the amplifier block 102, generates a residual analog signal in the amplifier 215 which, after amplification, would be suitable for use in the next stage of the pipeline. More specifically, in processing block 103, the input signal is converted into a 2-bit digital signal B0, B1. The 2-bit digital signal B0, B1 is output to the digital block 130. Additionally, the 2-bit digital signal B0, B1 is used to control a digital-to-analog converter (in processing block 103), which supplies an analog signal corresponding to the converted value to a second input terminal of the amplifier block 102. Since the amplifier block 102 accepts a differential input signal in which the magnitude of the input signal is the voltage difference between the two inputs, the amplifier block receives at its inputs what is known in the art as the residual signal (i.e., the original signal minus the converted value).

[0008] Figs. 2A and 2B are block diagrams of the amplifier block 102, which illustrate the amplifier block 102 as comprising a switched capacitor amplifier 210 (Fig. 2A) and a common mode feedback circuit 250 (Fig. 2B). The switched capacitor amplifier 210 is a network comprising a pair of input terminals 211a, 211b, respectively for a differential input signal comprising signals Vinp (coupled to the Vin signal) and Vinn (coupled to the output signal from processing block 103); a pair of input terminals 211c, 211d respectively for a differential reference signal comprising signals Vrefp, Vrefn; input terminal 211e for a common mode voltage reference signal Vcm (in the middle of the power supply range); switches 212a and 212b respectively controlled by clock signals $\phi 1$ and $\phi 2$; capacitors 213a, 213b, 214a, 214b; nodes A, B, and C; amplifier 215; and output terminals 216a and 216b, respectively for a differential output signal comprising signals Voutn and Voutp, arranged as shown. Switches 212a are closed

when clock signal $\phi 1$ is high and open when clock signal $\phi 1$ is low. Similarly, switches 212b are closed when clock signal $\phi 2$ is high and open when clock signal $\phi 2$ is low. The relationship between clock signals $\phi 1$ (high during a sampling phase of the ADC) and $\phi 2$ (high during a conversion phase of the ADC) is shown in Fig. 3. Typically, capacitors 213a and 213b are identical, and 214a and 214b are also identical.

[0009] The common mode feedback circuit 250 includes input terminal 251 for receiving the common mode voltage Vcm; input terminal 216 for receiving a bias voltage Vbias; switches 252a and 252b which are respectively controlled by clock signals $\phi 1$ and $\phi 2$; capacitors 253-256; and nodes A, B, and C, respectively coupled to corresponding nodes of the switched capacitor amplifier 210. Switches 252a are closed when clock signal $\phi 1$ is high and open when clock signal $\phi 1$ is low. Similarly, switches 252b are closed when clock signal $\phi 2$ is high and open when clock signal $\phi 2$ is low.

[0010] The processing performed in the processing block 103 is primarily digital processing and little power is wasted there. However, the processing performed in the amplifier block is analog processing, and as described below, wasteful in power consumption.

[0011] While clock $\phi 1$ is high, in addition to the above-described processing performed by the processing section 103, the differential input signals at the amplifier block 102, i.e., signals Vinp and Vinn, are respectively sampled by input capacitors 213a, 213b. Additionally, a common mode voltage Vcm is supplied to the opposite side of each capacitor. The common mode voltage Vcm is typically set to the average value between the voltage levels of the two power supply rails. That is, if one power supply rail is ground and another is 5 volts, Vcm would be 2.5 volts. During this phase, the amplifier 215 is idle, and the outputs Voutn, Voutp of the amplifier 215 are shorted to each other. Outputs Voutn, Voutp are each maintained at a voltage level equal to the

common mode voltage Vcm via the common mode feedback circuit 250. Once adequate time has elapsed to permit capacitors 213a, 213b, 214a, 214b to sample the input signals Vinp, Vinn, the clock signal $\phi 1$ goes low and the sampling phase ends.

[0012] At the same time, clock signal $\phi 2$ goes high, to indicate the start of the conversion phase. During this phase, no processing is performed by the processing section 103. However, in amplifier block 102, capacitors 213a, 213b are coupled as inputs to the amplifier 215 and capacitors 214a, 214b, are connected to provide negative feedback across amplifier 215. The amplifier 215 produces an output signal comprising signals Voutn, Voutp in accordance with equation (1) below:

[0013] (1) $$(Voutp - Voutn)/(Vinp - Vinn) = (1 + (Cin/Cfb)),$$

where Cin is the capacitance of a input capacitor, such as capacitor 213a, and Cfb is the capacitance of a feedback capacitor, such as capacitor 214a. Since each stage of the ADC 100 is responsible for ultimately converting 1-bit of the entire analog-to-digital processing, a gain of 2.0 is desired (since each bit differs in magnitude from the next bit by a factor of 2). Typically, this is achieved by setting Cin equal to Cfb.

[0014] One problem associated with the above described operation is that each stage 101 of the analog to digital converter 100 is operated in a manner which wastes power. More specifically, in each stage 101, the amplifier 215 is idle during the sampling phase but still consumes bias current. Additionally, during the sampling phase, the outputs of the amplifier 215 are shorted together. As a result, during the conversion phase, the outputs of the amplifier must slew from the common mode voltage (Vcm) to the appropriate voltage. This slewing between the common mode and required voltage further increases power consumption and affects accuracy of settling time.

[0015] Accordingly, it would be advantageous to increase power efficiency and improve operation an analog to digital converter.

SUMMARY OF THE INVENTION

[0016] The present invention is directed to improving the efficiency and throughput of an analog to digital converter. More specifically, the amplifier block for each stage of an analog to digital converter is provided with a switching network for implementing a double sampling and double conversion analog to digital converter stage. Rather than using one phase of a clock cycle for sampling and another for conversion, the both phases of the clock are used for sampling and conversion. By also using two independent processing blocks per stage, the analog to digital converter of the invention can achieve double throughput for approximately the same level of power consumption as with a conventional analog to digital converter. Alternatively, throughput may be maintained at the same level as that of a conventional analog to digital converter. This permits reducing the gain bandwidth of the amplifier blocks in the invention by about half, thereby affecting a power reduction in comparison with the conventional analog to digital converter. Additionally, the output signal of the amplifier itself is not reset to a common mode voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of exemplary embodiments of the invention given below with reference to the accompanying drawings, in which:

[0018] Fig. 1 is a block diagram of a conventional pipelined analog-to-digital converter;

[0019] Figs. 2A and 2B are schematic circuit diagrams of one of the amplifier blocks of Fig. 1, including the switched capacitor amplifier (Fig. 2A) and the common mode feedback circuit (Fig. 2B);

[0020] Fig. 3 is a timing diagram illustrating the relationship between clock signals in Figs. 1, 2A, and 2B;

[0021] Fig. 4 is a block diagram of a pipelined analog-to-digital converter in accordance with an exemplary embodiment of the invention;

[0022] Figs. 5A and 5B are schematic circuit diagrams of a switched capacitor amplifier and its associated common mode feedback circuit, respectively, in one of the amplifier blocks of Fig. 4; and

[0023] Fig. 6 is a block diagram of a processor based system having an integrated circuit with the ADC of Fig. 4.

DETAILED DESCRIPTION OF THE INVENTION

[0024] The ADC 400 of the exemplary embodiment shown in Fig. 4 include amplifier blocks 102' that operate continuously. This is achieved by providing the ADC 400 with two input analog signal streams (Vina, Vinb) to convert into two corresponding digital output signals. As shown in Fig. 4, the two analog input signal streams (Vina, Vinb) are combined in a time multiplexed fashion to form a single input signal, which is presented as a differential signal having components Vinp, Vinn to the

input signal pins 150a, 150b. Similarly, the two digital output signals Bit1a, Bit2a, ... , BitNa and Bit1b, Bit2b, ..., BitNb are output from two digital blocks 130a, 130b as described below.

[0025] Now referring to the drawings, where like reference numerals designate like elements, Fig. 4 shows a block diagram of the pipelined ADC 400. ADC 400 can include the same clock generator 110 and reference voltage generator 120 as ADC 100 (Fig. 1). Thus, the reference voltage (Vref) and clock signals (ϕ1, ϕ2) can operate as in ADC 100.

[0026] During each phase of operation, each stage 101' accepts an input signal and outputs an output signal. The stages 101' are cascaded, so that the first stage 101' accepts an input signal at terminal 150 and outputs a signal which becomes the input signal for the next stage 101'. Each stage 101' can be similar to stage 101 of ADC 100. However, in each stage 101' there are two processing blocks 103a, 103b, and as described below in connection with Figs. 5A and 5B, the circuitry of amplifier block 102' is different from that of amplifier block 102 of ADC 100.

[0027] Each processing block 103a and 103b can have the same circuitry, and perform the same function, as processing block 103 of ADC 100. However, processing block 103a performs its function with respect to the first input signal stream Vina while processing block 103b performs its function with respect to the second input signal stream Vinb. Since the two input signal streams Vina, Vinb are time multiplexed (e.g., a signal from stream Vina is presented at inputs 150a, 150b when clock ϕ1 is high, while a signal from Vinb is presented at inputs 150a, 150b when clock ϕ2 is high), processing block 103a is clocked to perform its sampling phase when clock signal ϕ1 is high, while processing block 103b is clocked to perform its sampling phase when clock signal ϕ2 is high. Similarly, associated with the processing blocks 103a is a digital block 130a, and associated with processing blocks 103b is a digital block 130b. Digital blocks 130a and

130b have the same circuitry, and perform the same function, as processing block 130 of ADC 100. Thus, digital block 130a output signals Bit1a, Bit2a, ... , BitNa from signals B0a, B1a from the plurality of processing blocks 103a while digital block 130b output signals Bit1b, Bit2b, ..., BitNb from signals B0b, B1b from the plurality of processing blocks 103b.

[0028] Figs. 5A and 5B are block diagrams of the amplifier block 102', which illustrate the amplifier block 102' as comprising a switched capacitor amplifier 210' (Fig. 2A) and a common mode feedback circuit 250' (Fig. 2B). The switched capacitor amplifier 210' is a network comprising a pair of input terminals 211a, 211b, respectively for a time-multiplexed differential input signal comprising signals Vinp, Vinn; two pairs of input terminals 211c, 211d respectively for a differential reference signal comprising signals Vrefp, Vrefn; input terminals 211e for a common mode voltage reference signal Vcm; switches 211a and 211b respectively controlled by clock signals ϕ1 and ϕ2; capacitors 213a, 213b, 214a, 214b; nodes A, B, and C; amplifier 215; and output terminals 216a and 216b, respectively for a time multiplexed differential output signal comprising signals Voutn and Voutp, arranged as shown. The signals on output terminals 216a and 216b are provided as input to the next stage 101'. The fully differential circuitry of Fig. 5A rejects common mode noise. Switches 212a are closed when clock signal ϕ1 is high and open when clock signal ϕ1 is low. Similarly, switches 212b are closed when clock signal ϕ2 is high and open when clock signal ϕ2 is low.

[0029] The common mode feedback circuit 250', which corrects imbalance in common mode voltage, includes input terminals 251 for receiving the common mode voltage Vcm; input terminals 216 for receiving a bias voltage Vbias; switches 252a and 252b which are respectively controlled by clock signals ϕ1 and ϕ2; capacitors 253-256; and nodes A, B, and C, respectively coupled to corresponding nodes of the switched capacitor amplifier 210'. Switches 252a are closed when clock signal ϕ1 is high and

open when clock signal $\phi 1$ is low. Similarly, switches 252b are closed when clock signal $\phi 2$ is high and open when clock signal $\phi 2$ is low. In one exemplary embodiment, capacitors 254-255 were each 0.03 pico-farad capacitors while capacitor 253, 256 were each 0.1 pico-farad capacitors.

[0030] The processing performed in the amplifier block 102' in the switched capacitor amplifier 210' and common mode feedback circuit 250' can be understood from the above description of operations of amplifier block 102 (Fig. 1). However, the use of two separate input/output networks permits the two networks to be respectively controlled by clock signals $\phi 1$ and $\phi 2$. More specifically, when $\phi 1$ is high and $\phi 2$ is low, one network is formed by closing switches 212a and 252a and opening switches 212b and 252b. While $\phi 1$ is low and $\phi 2$ is high, the other network is formed by closing switches 212b and 252b and opening switches 212a and 252a.

[0031] Thus, while each network still alternates between the sampling phase and the conversion phase, the two networks are out of phase by the difference between the two clock signals $\phi 1$ and $\phi 2$, and thus, the shared amplifier 215 is never idle. In contrast to a single sampling and single conversion technique, where the shared amplifier 215 spends approximately half its time idling while consuming power by using DC bias current, in the exemplary embodiment the current draw remains the same. Thus, if the clocks $\phi 1$ and $\phi 2$ were maintained at the same rate as a clock signal for a single sampling and single conversion, the amplifier of Figs. 4, 5A, and 5B would have double throughput while drawing approximately the same amount of power. Alternatively, the clocks $\phi 1$ and $\phi 2$ can be reduced in frequency by 50% relative to a single sample single conversion amplifier, and thus maintain the same throughput. However, in this scenario the required gain-bandwidth of the amplifier is also cut by half, thereby reducing power consumption by half as well. Thus, the amplifier of Figs. 4, 5A, and 5B may be used in at least two manners to reduce power consumption by approximately half.

[0032] Fig. 6 illustrates a processor based system 600 having an integrated circuit 601 including the ADC 400 of Fig. 4. In particular, the integrated circuit 601 may include a CMOS imager (not illustrated), and the imager may include two ADCs to increase throughput. The system 600 further includes a memory device 602, a processor 603, and a peripheral 604. Each of these components are coupled to a bus 610. The processor based system may include additional devices, and may be a portable consumer electronics device, such as a digital camera, cellular telephone, pacemaker, defibrillator, toy, or other battery-operated device.

[0033] While the invention has been described in detail in connection with exemplary embodiments, it should be understood that the invention is not limited to the above disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alternations, substitutions, or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not limited by the foregoing description or drawings, but is only limited by the scope of the appended claims.